

What is claimed is:

- 1 1. A bit line contact structure, comprising:
2 a substrate having a transistor thereon, the transistor
3 having a gate electrode, drain region, and source
4 region;
5 a composite dielectric layer, sequentially having a
6 first dielectric layer, barrier layer, and second
7 dielectric layer, blanketly formed on the
8 transistor, the first dielectric layer comprising
9 a spin-coating material, the composite dielectric
10 layer having an opening exposing the drain
11 region; and
12 a conductive layer in the opening.
- 1 2. The structure as claimed in claim 1, wherein the
2 first dielectric layer comprises polyimide,
3 polysilsequioxane, or fluorinated polyimide.
- 1 3. The structure as claimed in claim 1, wherein the
2 first dielectric layer is about 3000Å to 4000Å thick.
- 1 4. The structure as claimed in claim 1, wherein the
2 barrier layer is SiN.
- 1 5. The structure as claimed in claim 1, wherein the
2 barrier layer is about 100Å to 300Å thick.
- 1 6. The structure as claimed in claim 1, wherein the
2 second dielectric layer comprises an oxide layer.

1 7. The structure as claimed in claim 1, wherein the
2 second dielectric layer is about 1000Å to 3000Å thick.

1 8. The structure as claimed in claim 1, wherein the
2 conductive layer is doped polycrystalline silicon, tungsten,
3 aluminum, or copper.

1 9. The structure as claimed in claim 1, wherein the
2 first conductive layer is about 2000Å to 4000Å thick.

1 10. A method of fabricating a bit line contact
2 structure, comprising:

3 providing a substrate having a transistor thereon, the
4 transistor having a gate electrode, drain region,
5 and source region;

6 blanketly forming a first dielectric layer on the
7 transistor using spin coating;

8 conformally forming a barrier layer covering the first
9 dielectric layer;

10 blanketly forming a second dielectric layer on the
11 barrier layer;

12 planarizing the barrier layer;

13 forming a patterned resist layer on the second
14 dielectric layer;

15 etching the second dielectric layer using the patterned
16 resist layer as an etching mask, forming an
17 opening exposing the barrier layer;

18 removing the patterned resist layer;

19 removing the barrier layer in the opening;

20 etching the first dielectric layer using the second
21 dielectric layer as an etching mask, forming a
22 via; and
23 filling the via with a conductive layer.

1 11. The method as claimed in claim 10, further
2 comprising removing the patterned resist layer using ashing.

1 12. The method as claimed in claim 10, wherein the
2 first dielectric layer comprises polyimide,
3 polysilsequioxane, or fluorinated polyimide.

1 13. The method as claimed in claim 10, wherein the
2 first dielectric layer is about 3000Å to 4000Å thick.

1 14. The method as claimed in claim 10, wherein the
2 conductive layer is doped polycrystalline silicon.

1 15. The method as claimed in claim 10, wherein the
2 conductive layer is tungsten, aluminum, or copper.

1 16. The method as claimed in claim 10, wherein the
2 conductive layer is about 2000Å to 4000Å thick.

1 17. The method as claimed in claim 10, wherein the
2 barrier layer is SiN.

1 18. The method as claimed in claim 10, wherein the
2 barrier layer is about 100Å to 300Å thick.

1 19. The method as claimed in claim 10, wherein the
2 second dielectric layer comprises an oxide layer formed by a
3 precursor having at least tetra ethoxysilane (TEOS).

1 20. The method as claimed in claim 10, wherein the
2 second dielectric layer is initially about 3000Å to 6000Å
3 thick.

1 21. The method as claimed in claim 10, wherein
2 planarizing the second dielectric layer uses chemical
3 mechanical polishing (CMP), leaving the second dielectric
4 layer about 1000Å to 3000Å thick.

1 22. The method as claimed in claim 10, wherein etch
2 selectivity of the first dielectric layer with respect to
3 the gate electrode is reaching approximately 30 or greater.

1 23. The method as claimed in claim 10, wherein the
2 gate electrode further comprises a spacer overlying a
3 sidewall thereof.

1 24. The method as claimed in claim 10, wherein the
2 spacer is SiN.